IN THE CLAIMS

Kindly replace the claims of record with the following full set of claims:

1. (Currently amended) A video circuit for processing video signals which show images on a display panel with linear light transition, comprising a gamma correction circuit, a quantizer and a sub-field generator circuit, wherein a coarse adjustment of the quantization is made in a first random-access memory and a fine adjustment of the quantization is made in a second random-access memory, wherein elements of each of said first and second memories represent absolute values associated with neighboring pixels by which a quantization error is determined at a current pixel value.

2. (Currently amended) A video circuit for processing video signals which display images on a display panel with linear light transition, comprising a gamma correction circuit, a quantizer and a sub-field generation circuit, wherein most significant bits are quantized in a first random-access memory and least significant bits are quantized in a second random-access memory, wherein elements of each of said first and second memories represent absolute values associated with neighboring pixels by which a quantization error is determined at a current pixel value.

3. (Currently amended) A video circuit for processing video signals which show images on a display panel with linear light transition, comprising a gamma correction means, a quantization means and a sub-field generation means wherein the quantization means is a random-access memory, wherein elements of said memory representing absolute values associated with neighboring pixels by which a quantization error is determined at a current pixel value.

4. (Previously presented) A video circuit as claimed in claim 3, wherein the random-access memory additionally performs dequantization.

5. (Previously presented) A video circuit as claimed in claim 3 wherein the random-access memory is said gamma correction means.

6. (Previously presented) A video circuit as claimed in claim 4, wherein an inverse gamma circuit is arranged downstream of the random-access memory.

7. (Previously presented) A video circuit as claimed in claim 3, wherein the random-access memory is said sub-field generation means.

8. (Previously presented) A video circuit as claimed in claim 7, wherein sub-field generation values are applied to a filter via a conversion means and a dequantization means.

9. (Previously presented) A video circuit as claimed in claim 8, wherein the filter applies values to an adder which is situated in an input area of a second signal which represents pixel values of a neighboring line.

10. (Previously presented) A video circuit as claimed in claim 9, wherein sub-field generation values are applied to the adder via a second conversion means and a second dequantization means.

11. (Previously presented) A video circuit as claimed in claim 9, wherein pixel values of the neighboring line are quantized in a quantization means and subs-fields are generated in a further sub-field generation means wherein a further random access memory is said further quantization means and said further sub-field generation means.

12. (Cancelled).